OPERATING AND MAINTENANCE INSTRUCTION MANUAL

MODEL 235

AM BROADCAST AUDIO PROCESSOR

INOVONICS
INCORPORATED

— USER'S RECORD —
Model 235 - Serial No. ______
Date Purchased ___________
Warranty Card Mailed — ☐

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AM BROADCAST AUDIO PROCESSOR

March, 1999

INOVONICS INCORPORATED

1305 Fair Avenue • Santa Cruz, CA 95060
TEL: (831) 458-0552 • FAX: (831) 458-0554
Visit our Website: www.**inovon**.com

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Section I

INTRODUCTION

MODEL 235 PRODUCT DESCRIPTION

Historical Inovonics introduced its *Model 222 "NRSC" Processor* in 1987. This product was developed to meet certain "AM improvement" needs and became a very popular addition to existing audio processing systems in broadcast markets of all sizes. The NRSC fixed pre-emphasis and low-pass cutoff characteristics suggested in 1987 were subsequently mandated by the U.S. Federal Communications Commission.

General The 235 incorporates these same pre-emphasis and high-frequency-cutoff characteristics to meet NRSC requirements, but its expanded functions also include comprehensive program dynamics processing to maximize perceived loudness and to fully utilize the modulation capability of modern AM broadcast transmitters.

The 235 combines AGC, 3-band compression, low and high frequency equalization, and tight control over program peaks with a combination of hard limiting and judicious waveform clipping. Dynamics processing is followed by an overshoot-compensated low-pass filter exceeding NRSC specifications. The filter may be factory-tailored for other cutoff frequencies to accommodate European medium-wave transmissions or various international short-wave services.

Processing parameters are easily set with front-panel controls, or may be controlled from a remote location using the built-in RS-232 control bus and an IBM-compatible computer or modem interface.

Features To recap, features of the Inovonics 235 include:

- Comprehensive dynamic range processing which combines:
  - — Gated, "gain-riding" AGC
  - — 3-band average level compression
  - — Low- and high-frequency program equalization
  - — Asymmetrical peak limiting with selectable clipping depth.
- Low-pass filtering to the NRSC specification with patented filter overshoot compensation. Alternative cutoff frequencies can be provided.
- Easy front-panel control of processing parameters, or full computer control via RS-232 bus..

MODEL 235 TECHNICAL SPECIFICATIONS

Frequency Response (NRSC version)**:**
PROOF: ±0.25dB, 50Hz to 20kHz
OPERATE: ±0.5dB, 50Hz to 9.7kHz. Follows NRSC pre-emphasis and cutoff characteristics.

Distortion:
<1% THD at any PROGRAM DENSITY setting, and at PEAK PROCESSING settings which maintain negligible clipping depth.

Noise:
Better than 60dB below 100% carrier modulation (taken through NRSC de-emphasis network).

Gated AGC:
UK/EBU quasi-peak "PPM" response to program material; slow, 0.5dB-per-second correction rate over ±10dB range. Frequency-weighted gating threshold set at –25dB, referred to corrected input "zero" level.

Triband Compressor:
Second-order band-pass function; crossovers at 250Hz and 2.5kHz. Attack and release timing optimized for each band. PROGRAM DENSITY controls timing and inter-band "blending".

Fixed Pre-Emphasis:
The standard (US) version follows the "truncated" 75µs curve specified by the NRSC transmission standard. Alternative versions employ pre-emphasis appropriate to the specified cutoff frequency.

Variable Equalization (see Figures 2 and 3 on Page 5)**:**
HF: –3dB, 0dB (NRSC), +3dB, +6dB, +9dB; variable EQ curves are in addition to the NRSC or alternative fixed pre-emphasis.
LF: –9dB, –6dB, –3dB, 0dB (flat), +3dB.

Peak Controller:
Asymmetrical fast peak limiter integral with hard peak clipper. PEAK PROCESSING controls release timing and program-dependent clipping depth.

Low-Pass Function:
Phase-corrected, 9-pole FDNR active-elliptic filter with proprietary overshoot compensation. Exceeds NRSC requirements. (See Figure 1 on Page 5.)

Input:
Active-balanced, bridging; accepts nominal program line levels between –15dBu and +15dBu.

Output:
Active-balanced, 200-ohm resistive source; delivers 0dBm to +15dBm into a 600-ohm load.

Output Asymmetry:
Positive peak amplitude may be adjusted between 100% and 125% of the negative peak value.

Remote Control Provision:
RS-232 serial data port (DB-9 connector) allows all processing presets to be programmed or updated by an IBM-compatible computer. Necessary software is included.

Power Requirements:
105–130VAC or 210–255VAC, 50/60Hz; 15 watts.

Size and Weight:
1¾"H x 19"W x 10"D (1U);
10 lbs. (shipping).

Figure 1 - NRSC Cutoff Characteristic

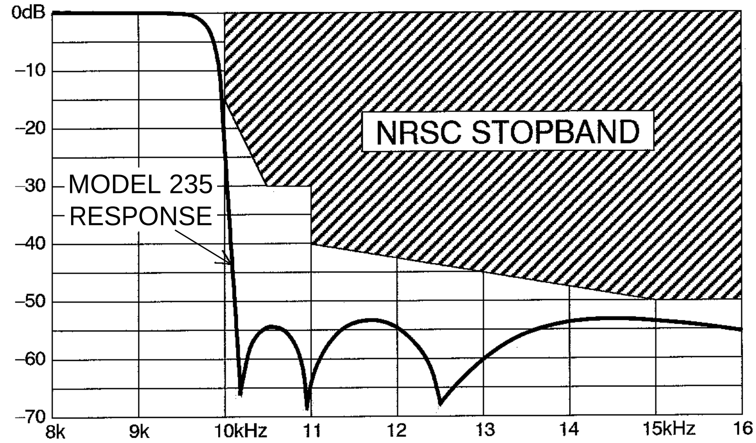


Figure 2 - LF Equalization Range (dashed line represents subsonic high-pass function)

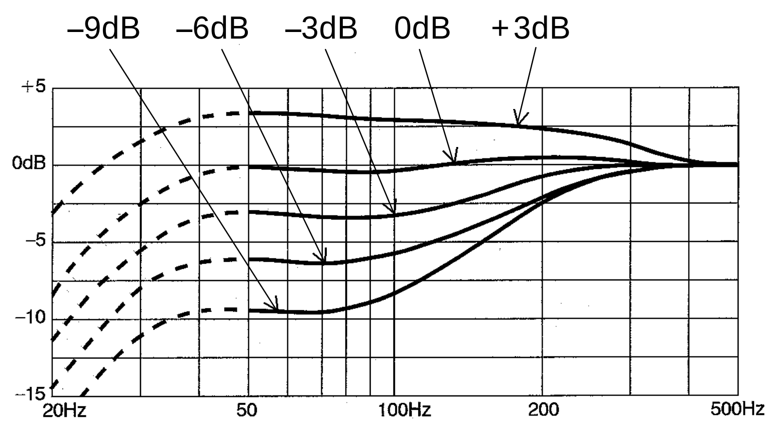
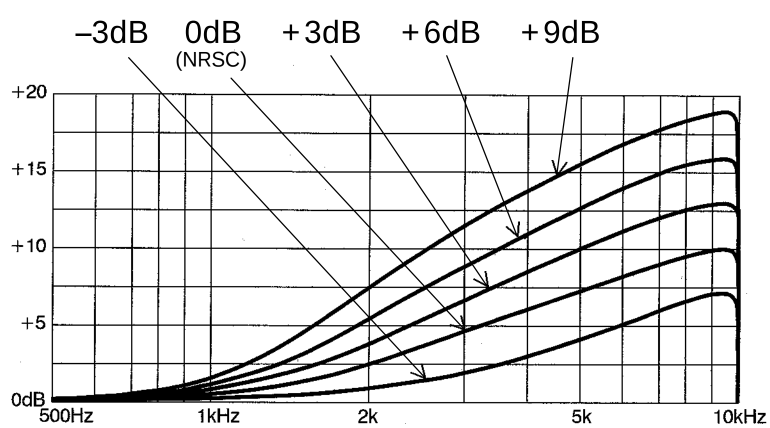


Figure 3 - HF Equalization Range ("0dB" represents NRSC fixed pre-emphasis)



BLOCK DIAGRAM

A simplified Block Diagram of the Model 235 is shown in Figure 4, below. Processor circuitry is detailed in the Circuit Descriptions section beginning on Page 17. These descriptions reference Schematic Diagrams found in the Appendix.

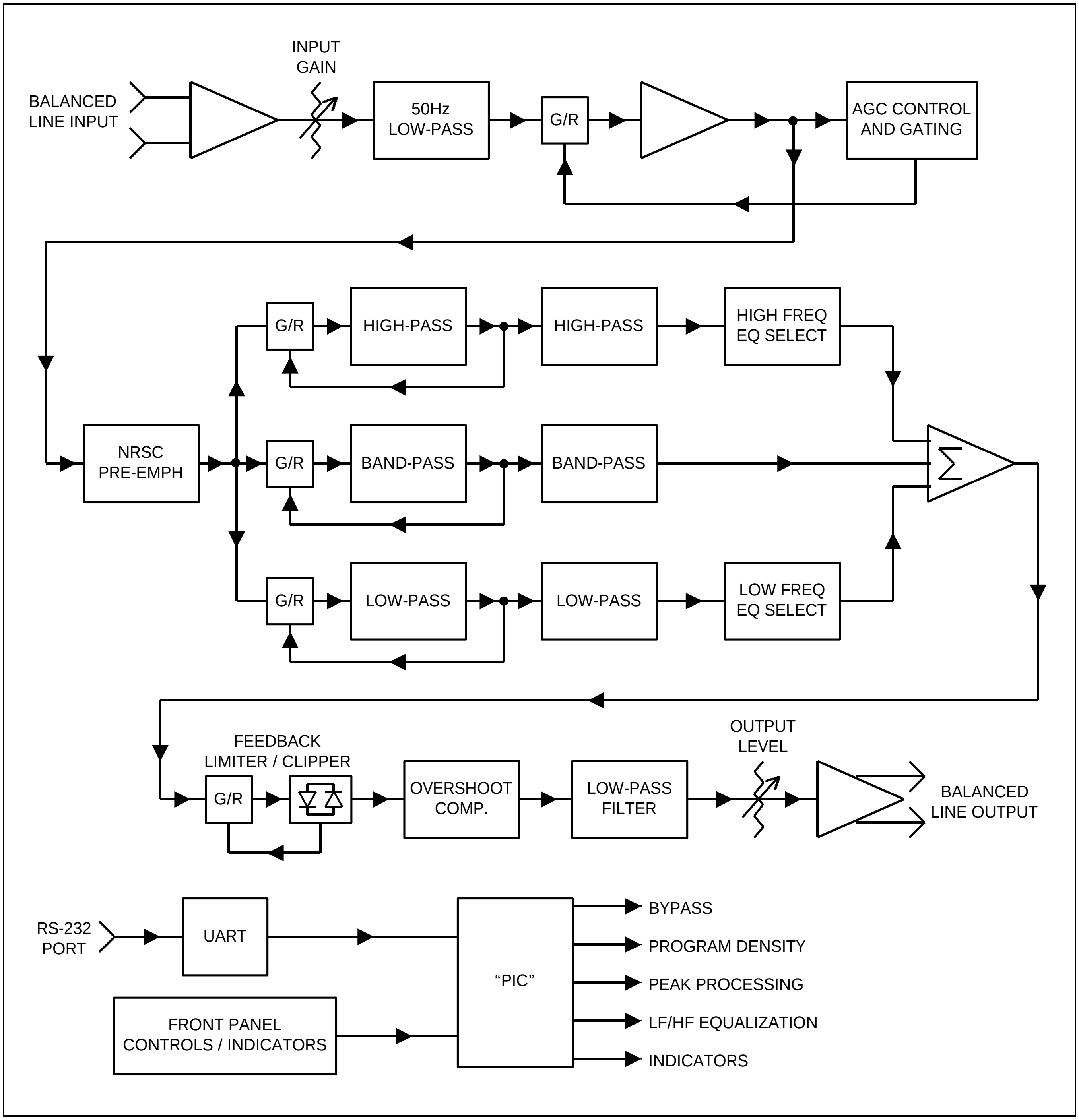


Figure 4 - Block Diagram, Model 235 AM Broadcast Audio Processor

Section II

INSTALLATION

UNPACKING AND INSPECTION

Immediately upon receipt of the equipment, inspect carefully for any shipping damage. If damage is suspected, notify the carrier at once, then contact Inovonics.

We recommend that you retain the original shipping carton and packing materials for return or reshipment, if necessary. In the event of return for Warranty repair, shipping damage sustained as a result of improper packing for return *may invalidate the Warranty!*

IT IS VERY IMPORTANT that the Warranty Registration Card found at the front of this Manual be completed and returned. Not only does this assure coverage of the equipment under terms of the Warranty, and provide some means of trace in the case of lost or stolen gear, but the user will automatically receive specific SERVICE OR MODIFICATION INSTRUCTIONS should they be issued by Inovonics.

MOUNTING

Rack Requirement The Model 235 mounts in a standard 19-inch equipment rack and requires only 1¾ inches (1U) of vertical rack space. Plastic "finishing" washers are recommended to protect the painted finish around the mounting holes.

Heat Dissipation Consuming less power than a counter-top coffee grinder, the 235, itself, generates negligible heat. The unit is specified for operation within an ambient temperature range extending from freezing to 120°F/50°C. But because adjacent, less efficient equipment may radiate substantial heat, be sure that the equipment rack is adequately ventilated to keep its internal temperature below the specified maximum ambient.

AC (MAINS) POWER

As delivered Unless specifically ordered for export shipment, the Model 235 is set at the factory for operation from 115V, 50/60Hz AC mains. The rear-panel designation next to the fuseholder will confirm both the mains voltage selected and the value of a proper fuse.

Voltage Selector A mains voltage selector switch is located beneath the top cover of the unit, close to the AC mains connector on the main circuit board. *With primary AC power disconnected*, slide the red actuator with a small screwdriver so that the proper mains voltage designation (115 or 230) shows. Be certain always to install an appropriate fuse, and check that the rear-panel voltage/fuse designation is properly marked. It is factory practice to cross-out the *inappropriate* designation with an indelible black marking pen. You can remove this strikethrough with lacquer thinner to redesignate.

BE SURE that the mains voltage selector setting and primary fuse value are appropriate for the mains supply before plugging the 235 Processor into the wall outlet.

Power Cord The detachable IEC-type power cord supplied with the Processor is fitted with a North-American-standard male plug. Nevertheless, the individual cord conductors are *supposed* to be color-coded in accordance with CEE standards; that is:

BROWN = AC “HOT” BLUE = AC NEUTRAL GRN/YEL = GROUND

If this turns out *not* to be the case, we offer our apologies (cords come from many sources) and advise that US color coding applies:

BLACK = AC “HOT” WHITE = AC NEUTRAL GREEN = GROUND

RADIO FREQUENCY INTERFERENCE (R F I)

Location Although we have anticipated that the 235 will frequently be installed adjacent to high-power AM transmitters, please practice care and common sense in locating the unit away from *abnormally* high RF fields.

Ground Loops Because the input and the output of the Model 235 are chassis-ground-referenced, a mains frequency or RF ground loop could be formed between the input or output cable shield grounds and the AC power cord ground. A “ground-lifting” AC adapter will probably remedy such a situation, though the chassis somehow must be returned to earth ground for safety. Generally, being screwed-down in the equipment rack will satisfy the safety requirement.

LINE INPUT AND INPUT RANGE SELECTION

Input Connection The Model 235 has an electronically-balanced (transformerless) program LINE INPUT. This is brought out to a screw-terminal barrier strip on the rear panel, and includes a chassis ground connection for the input cable shield. *Please note that the screw-terminal barrier block can be unplugged from the chassis, simply by pulling it straight out!*

This makes connection a bit easier and allows quick removal of the 235 from the rack should maintenance ever be required.

Balanced Input

A balanced program audio feed to the 235 Processor will use both the + and the – terminals, plus the associated G (ground). Since this is a bridging (high impedance) input, it does not provide a 'termination' for the console or other equipment which feeds the Processor. Should you feel so compelled, you may connect a 600-ohm resistor across the + and – input terminals, though the concept of 600-ohm "line matching" dates from the age of transformer coupling and the mystique of telephone lines with characteristic impedance.

Unbalanced Input

In an isolated rare instance, the 235 might be fed from "semi-pro" gear with an unbalanced output. In such an unlikely case, the single center conductor of the shielded input lead should be connected to the + terminal, and the shield to G. In addition, a jumper wire should be installed between the – terminal and G.

Input Gain Range

The Model 235 Processor can accommodate line-level program input with a nominal "Zero-VU" value between –15dBu and +15dBu. This 30dB range is divided into two, more manageable 15dB ranges with an internal jumper.

As shipped, the 235 is jumpered for professional level inputs between 0dBu and +15dBu. Most console and STL outputs fall into this range, +4dBu, +6dBu and +8dBu being typical levels.

Lower levels, between –15dBu and 0dBu, may be encountered with interfacing with "semi-pro" gear, or with feeds from leased telephone circuits. The extra gain for the low level range is enabled by changing a jumper beneath the top cover.

Gain Jumper

The input range jumper strip is located just behind the LINE INPUT connector and identified as "JMP1" in the circuit board legend. The jumper has an H and an L marking to indicate the proper jumper placement for High level and for Low level inputs, respectively. Figure 5 illustrates these jumpering options.

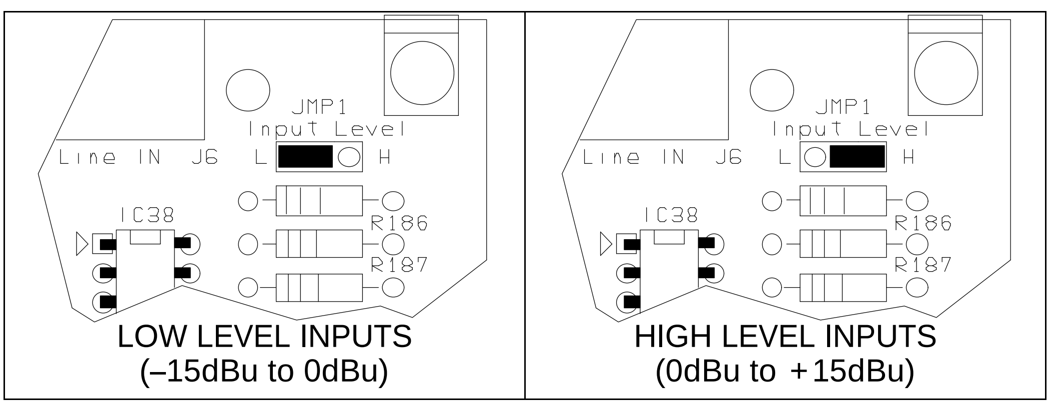


Figure 5 - LINE INPUT Range Selection

PROGRAM LINE OUTPUT

The only guarantee of protection against transmitter overmodulation is a short and direct connection between the output of the Model 235 Processor and the transmitter input. Any frequency or phase error between the Processor and transmitter will partially (or completely!) negate the tight final peak control which the 235 provides.

This means that the 235 must be located *at the transmitter site* to be completely effective. Even a digital link (STL, ISDN, FRAC-T1 or FDIC) will compromise the peak control function. Moreover, the interconnect cable should be kept short and direct. Less than 10 feet of a shielded, twisted pair is preferred.

Output Connection and Signal Phase

The LINE OUTPUT of the 235 Processor terminates at the removable barrier strip on the rear panel. This output is electronically-balanced (transformerless) and *must be connected to the input of the transmitter with proper regard to signal phase.*

Output terminals are marked + and –. These should be connected to similarly-marked transmitter input terminals. The output program signal from the 235 will exhibit waveform asymmetry in the direction indicated; that is, the + terminal will be (additionally) positive-going with (increased) positive peaks. Make sure that the + terminal is connected to the transmitter input terminal which yields an increase in carrier level for a positive signal excursion.

REAR-PANEL “MODE” SWITCH

The 3-position toggle switch on the rear panel of the 235 selects OPERATE, for local (front-panel) operation, REMOTE CONTROL, for processor control by computer or modem through the RS-232 port, and PROOF, which effectively bypasses the unit.

The switch must be left in the OPERATE position if front-panel buttons are to be used for setting processing parameters. Once set, the switch may be switched to REMOTE CONTROL position to lock-out the front panel buttons and protect Processor setup. When it is in the OPERATE position, the Processor *will not respond* to remote, RS-232 commands.

The switch must be set to REMOTE CONTROL to activate the RS-232 port for remote computer or modem control. See appropriate instructions for remote Processor operation beginning on Page 15.

PROOF completely bypasses the functions of AGC, compression, pre-emphasis, equalization, limiting, clipping and the low-pass output filter. It effectively turns the Processor into a line amplifier, though the subsonic, 50Hz high-pass function is still active.

Section III

SETUP AND OPERATION

OPERATIONAL OVERVIEW AND PANEL APPOINTMENTS

This section leads off with an overview of the 235 Processor with particular reference to front-panel indicators and controls. *All functions are described and explained in this overview.* Whether or not you believe in reading Manuals, please at least check these descriptions to verify that our terminology is in agreement with your understanding. If you call us (especially if you use our toll-free number!) with a question that is answered here, we are likely to be very cross with you.

AGC

235 processing begins with slow, “gain-riding” Automatic Gain Control, or AGC. This is not considered a *dynamic* processing function because it does not alter program dynamics and contribute to perceived loudness. The purpose of the AGC is to erase *long-term* variations in the input program level and to present subsequent processing stages with a consistent program signal.

Input levels can wander up and down for a number of reasons. Among these are: 1) an operator’s lack of attention to manual gain-riding, 2) different interpretations of console level meter readings among board operators, or 3) the misrepresentation of the program signal waveform by the traditional, sluggish VU meter.

AGC in the 235 Processor is “gated.” It does not “hunt” or bring up background noise during pauses in the program. AGC gain freezes when midrange program energy falls below the preset gating threshold.

AGC response to the program waveform is quasi-peak-responding. Its 10-millisecond integration is similar to the *response* of a European Peak Program Meter. *Correction*, on the other hand, is slow: only 1dB every couple of seconds. This makes overall operation roughly equivalent to a human operator watching a PPM and sneaking the level up and down, slowly and unobtrusively.

AGC correction spans a 20dB range. The INPUT GAIN control is adjusted to center AGC action, effectively yielding a ±10dB correction window. AGC gain is metered by the associated bargraph display, and the bottom-most GATE OPEN indicator lights whenever the circuit senses legitimate program energy to enable circuit operation.

Plus AGC readings (+5, +10) indicate that the input signal is below the optimum level and that the circuit is slowly bringing the gain up. *Minus* readings (there are no such things as *negative* dBs, at least not in our space/time continuum) show that the input signal is too "hot" and that the level is being reduced to compensate.

COMPRESSION

The definition of *compression* generally acknowledges a reduction in the *average* dynamic range of a speech or music program signal. Program level is frequently (and sometimes erroneously) expressed in r.m.s. terms and is integrated over a period of a hundred milliseconds or more. A *compression ratio* may be expressed or implied, which might be on the order of 2:1 or 4:1, indicating a fractional output level change for a given input level variation.

The Model 235 compresses program dynamics in three frequency bands. These are labeled LOW, MID and HIGH. In the interest of maximizing perceived loudness, the compression ratio in each of these three bands is made uncommonly steep for a compressor, 20:1 or greater. Thus the circuit acts more like a 3-band *limiter* than a traditional *compressor*. Attack time within each band is quite rapid; release, on the other hand, is variable and a function of the PROGRAM DENSITY setting, which is explained in more detail under the next heading. The three COMPRESSION displays show dBs of gain reduction for each band.

PROGRAM DENSITY

Two up/down buttons allow the operator to choose eight relative degrees of density control. These are indicated on the adjacent LED bar display.

Set at (MIN), the 3-band compressor has a slow release to what we call a *platform* value. The platform is established by an average of the gain reduction in all three frequency bands. This platform causes the circuit to perform more like a single-band compressor, and spectral density of the processed program audio is only marginally effected.

As PROGRAM DENSITY is increased toward (MAX), the platform and the "blending" of the bands is reduced so that the full multiband advantage may be realized. Compressor release timing is progressively shortened as well, and this imparts a "busy" character to the program to further increase perceived loudness.

EQUALIZATION

In addition to NRSC (or alternative) fixed pre-emphasis, the 235 provides a range of control over both high- and low-frequency program equalization.

The effect of the equalizers is shown in Figures 2 and 3 on Page 5. The LOW FREQ. and HIGH FREQ. buttons cycle the

EQUALIZATION settings through the five choices for each end of the spectrum.

CLIP PEAK LIMIT

The final processing block of the 235 is a unique asymmetrical “feedback” peak-limiter/clipper. A final clipping circuit is able to monitor its own action and tell the limiter how hard to work, depending on how aggressively the PEAK PROCESSING (described next) has been set. This feedback technique establishes a stable and fixed *clipping depth*, or ratio between the two peak control functions. Two LEDs flash as circuitry copes with program peak excursions, enabling a visual interpretation of this limit-to-clip ratio.

PEAK PROCESSING

Two up/down buttons select eight levels of program peak control, indicated on the adjacent LED display. At the (MIN) setting, typical values of peak reduction are on the order of 5dB, and *no* clipping is allowed. Setting number 2 also restricts peak reduction to the same 5dB figure, but enables a small amount of clipping as well. From setting number 3 upward, peak reduction runs about 10dB, with clipping increasing as the setting approaches (MAX).

NOTE: Always pay particular attention to the effect of heavy peak processing on solo voices. Complex waveforms such as instrumental music can tolerate a good deal more clipping than solo vocals and voice announcements.

INPUT GAIN

Input sensitivity of the Processor is adjusted by this 15-turn potentiometer to accommodate varying input levels. The control itself has 15dB *continuous* adjustment. This, coupled with input level range jumpering (Figure 5, Page 9), accommodates the 235’s full 30dB input signal level range. The INPUT GAIN control is set so that normal program material keeps the AGC indicator close to center-scale.

OUTPUT LEVEL

This multi-turn control adjusts the Processor output level to match the input requirements of the transmitter. The pot is adjusted so that *negative* program peaks reach *nearly* 100% modulation, as indicated by the station Modulation Monitor.

POS. PEAKS

This adjusts Processor output asymmetry. It allows naturally-occurring *positive* program peaks to exceed the value of negative peaks. In the U.S., for example, the maximum instantaneous value of carrier amplitude is allowed to reach as much as two-and-one-half times the unmodulated (resting) carrier value. This condition is referred to as 125% *positive* modulation and references a maximum figure of 100% *negative* carrier modulation, or complete carrier cutoff.

POWER

Harmonically in accord with today’s humanity-based concepts of *nurturing* and *self-esteem*, Inovonics has included this special switch, the operation of which *emPOWERs* the operator of the Processor to reach new heights in broadcasting *sustainability*. (?)

PROCESSOR SETUP PROCEDURE

This setup procedure assumes a typical, transmitter-site installation of the 235, with the LINE INPUT fed from the output of the console or from a telephone line or STL receiver.

At this point the Processor should be installed in the program chain with power applied. The OUTPUT LEVEL control should be turned fully counterclockwise.

Input Level Adjustment

The INPUT GAIN control is adjusted to center the AGC operating range with a nominal “Zero-VU” program line input. If the following procedure shows control range to be outside adjustment limits, recheck circuit board jumpering for *Input Gain Range* selection as described on Page 9.

1. Apply a 500Hz test tone from the console at a level one-and-one-quarter dB *above* normal reference level. This is simply a console VU meter indication of +1¼VU.
2. Adjust the INPUT GAIN control so that *both* the 0dB AGC GAIN indicator *and* the one just below it (–2.5dB) light equally. Remember that the AGC circuit responds very slowly to level change, so exercise patience in making this important adjustment.

Once the INPUT GAIN has been adjusted with a test tone, you can switch-over to normal program material. If the procedure has been performed properly, and if the board operator pays reasonable attention to the meter, AGC GAIN will nearly always remain between +5dB and –5dB.

Output Level Adjustment

Perform this part of the setup procedure “on air” under normal operating conditions and using typical program material. You must have access to the station’s Modulation Monitor and understand its operation.

1. Preset panel controls as follows:
   OUTPUT LEVEL — fully counterclockwise
   POS. PEAKS — fully counterclockwise
   EQUALIZATION — 0dB for both HIGH FREQ. and LOW FREQ.
   PROGRAM DENSITY — (MAX)
   PEAK PROCESSING — (MAX)
2. Advance the OUTPUT LEVEL control for *negative peak modulation* of 90% to 95% as indicated by the Mod-Monitor.
3. If permitted by local regulations, advance the POS. PEAKS control for *positive peak modulation* of as much as +125% as indicated by the Mod-Monitor.

Once these adjustments have been made, reduce the PROGRAM DENSITY and PEAK PROCESSING settings for a less aggressive "sound." These two parameters should be experimented with, and a final choice for the settings based on the collective decision of several station personnel.

Possible Problems

Maximum output asymmetry of the 235 Processor is about +130%. If you crank-up the POS. PEAKS and do not see a corresponding increase in positive modulation on the Mod-Monitor, here are a couple of things to check:

1. *The transmitter is not linear*, and thus incapable of extra positive modulation. If the transmitter is plate-modulated, the modulator tubes could be "soft" or the power supply inadequate to support positive peaks. If this is the case it is *best not to try* to obtain positive modulation in excess of +100%, because transmitter non-linearity will create spurious sideband energy which will violate the NRSC "Occupied Spectrum" limits.
2. *The Processor output could be wired backwards!* If you turn up the POS. PEAKS and see an increase in *negative* modulation on the Mod-Monitor, you are almost certainly assured of a turnover in the interconnection. Try reversing the + and – terminals, either at the output of the Processor end or at the input of the transmitter (but not both, for heaven's sake!) to see if proper behavior is restored.

REMOTE CONTROL OF THE MODEL 235

Computer and Modem Compatibility

Control software provided with the 235 is written in Visual Basic 5®. It runs only under Windows 95® or subsequent 32-bit versions of Microsoft's popular operating system for IBM-compatibles. The software enables remote control of the Processor, either from a computer connected directly to the 235, or via modem interface.

Any Hayes-compatible modem *should* permit remote computer control of the Processor over an intermediate dial-up telephone circuit. The compatibility issue will be one between the computer's own modem and the remote modem associated with the 235 Processor. With full compatibility between the two modems, the interconnection will appear transparent, allowing the software to give the same rapid and effective control over the processing parameters as if the computer were connected directly.

Interconnection

The 235 Processor is a data *output* device, thus the RS-232 SERIAL INTERFACE connector is a DB09 *female*. A standard serial interconnect cable may be used to directly connect the Processor to the computer's serial (COM) port. As the computer is classed as an *input* device, it will have either a DB09 or DB25 *male* connector. If necessary, you may use one of the common 25-pin to 9-pin "mouse" adapter/reducers.

The external modem, on the other hand, is a data *output* device and will have a DB09 or DB25 *female* connector. A custom cable will need to be purchased or constructed.

Schematic Sheet 4 on Page 32 diagrams the several options for interconnect cables between the Model 235 and computer or modem.

Section IV

CIRCUIT DESCRIPTIONS

This section details circuitry of the Inovonics Model 235 AM Broadcast Audio Processor. Circuit descriptions refer to four pages of Schematic Diagrams contained in the Appendix, Section V, Pages 29 through 32.

If you're looking for some sort of alignment procedure for the 235, forget it. There are no internal controls for any sort of calibration, the circuitry being rock-solid through impeccable design.

NAVIGATION

Schematic component reference designations have not been assigned in as haphazard a manner as they might at first appear. Instead of annotating the *schematic* in a logical sequence, we instead chose to designate the *components on the circuit board* following their physical placement, top-to-bottom, left-to-right. We expect this practice will prove useful when troubleshooting, making it easier to locate the physical part after analyzing the diagram.

The Model 235 schematic consists of three sheets which cover the main circuit board and the front-panel assembly. Main-board components begin with the number "1"; i.e.: R1, C1, IC1. Front-panel components are in the five-hundred series; i.e.: R501, S501.

The front-panel assembly interconnects with the main board using three short ribbon-cable jumpers. J2 on the main board mates with J502 on the panel assembly, J4 to J504, and J5 to J505.

INPUT STAGE (Schematic Sheet 1, Page 29)

Line Input Balancing

IC36B is an "active-balancing" stage for the program line input, affording good RF suppression and rejection of other, unwanted common-mode signals. When R183 is jumpered into the input network with JMP1, the Line Input accepts "High" program levels between 0dBu and +15dBu. For "Low" level inputs, between –15dBu and 0dBu, R183 is jumpered out of the circuit. Input range jumpering is described on Page 9.

High-Pass Subsonic Filter

IC37B performs the dual function of a variable-gain stage and a 50Hz high-pass filter. Assuming negligible musical content below 50Hz, we can maximize loudness and optimize transmitter modulation by attenuating program frequencies below 50Hz at a rate of 12dB-per-octave. Referring to Figure 2 on Page 5, the direct effect of this rolloff can be seen in the curve for 0dB, “flat” low-frequency equalization. Its effect at other equalization settings may be noted as well.

The feedback path of IC37B includes the front-panel INPUT GAIN control, R212. This pot affords the 15dB of continuous level adjustment within each jumpered input gain range.

The sinewave signal level at the output of IC37B which will maintain AGC gain at 0dB is –5dBu.

AGC AMPLIFIER (Schematic Sheet 1, Page 29)

Antediluvian Gain-Control Element Explained

The next paragraph details operation of the AGC amplification stage, but the gain-control technique used there is typical throughout the Model 235.

IC38B is a classic inverting op-amp, but with transistors Q35 and Q36 included in the input network. It is the *saturation resistance* property of these two transistors which is used to effectively shunt input signal *current* to ground, thus controlling the overall gain of this stage. The signal voltage swing, being electrically very close to a current summing node, is negligible, far below the $V_{CE(SAT)}$ of the bipolar NPN devices used here. The upside-down, back-to-back transistor hookup helps linearize the circuit for a low figure of distortion. Surprisingly, gain reduction vs. base current is a stable and predictable function.

If this circuit is unfamiliar to you, don’t feel bad. It is somewhat unconventional and dates from one of Inovonics’ first products developed in the early 1970s. It is also the subject of a patent, long since expired.

Rectifier and AGC Control

IC39B and IC40B, along with diodes CR27 and CR28, give full-wave peak rectification of the gain-controlled input signal. R197 and C67 yield the 10-millisecond-integration for AGC response to program material.

IC41B is a DC gain stage with a fixed offset. Its output sits at +1.5VDC when the program level from IC38B is exactly –5dBu. The output of IC41B is driven negative when the program exceeds –5dBu, and is driven positive when program level drops below –5dBu.

Let’s assume for the moment that the output of IC41B is routed through IC42A directly to IC41A, an inverting comparator with a reference voltage of +1.5V and a tiny bit of hysteresis. The output of IC41A is going to snap smartly to the positive rail when program audio rises above –5dBu, and to the negative rail when it falls below this level. This toggles analog switch IC42B which steers integrator IC40A.

The integrator is driven from its own output when the program level is too low, and from an inversion of its output when the level is too high. This gives a *logarithmic* voltage ramp which matches the *logarithmic* transfer function of the gain-control stage to yield a *linear* dB/second correction. The time constant of R173 and C58 determine the slow, unobtrusive, 0.5dB/second correction rate of the AGC.

AGC Gating

The level-corrected program signal is monitored by the gating amplifier, IC38A. This is a first-order, band-pass filter with –3dB points at 300Hz and 3kHz. The purpose of this frequency weighting is to favor legitimate program material, and neglect rumbles and hisses which might otherwise cause the AGC to bring these noises to annoying levels.

The band-passed program signal is rectified by CR23 and CR24, and sensed by comparator IC37A. The output of this IC sits at the positive supply rail until a program signal exceeds the gating threshold, at which point it toggles to the negative rail, lighting the GATE OPEN indicator and switching IC42A from NO (normally-open) to NC (normally-closed).

When the gate is open, IC42A feeds program-level-derived DC from IC41B to comparator IC41A. This enables AGC circuitry to correct input gain. When the program level drops below threshold and IC37A toggles low, the actual AGC gain-control voltage is instead presented to comparator IC41A. This causes AGC gain slowly to return to the 0dB, resting value.

TRIBAND COMPRESSOR (Schematic Sheet 1, Page 29)

Fixed Pre-Emphasis

C53 is in the input path of IC38A imparts the fixed, NRSC pre-emphasis to the program signal ahead of the 3-band compressor. The resultant increase in high frequency energy is kept in check by normal compressor action.

Band-Pass Compression

IC28B is a first-order band-pass stage defining a second-order response for the MID band. Gain control ahead of this stage gives a distortion-reduction advantage because the *compressed* signal is filtered. The MID band samples some energy in the adjacent bands which helps maintain a more uniform response under heavy compression to eliminate “phase-swishing” and other audible artifacts.

Gain stage IC29B feeds the full-wave rectifier comprised of Q26, Q27 and Q28. This simple, yet effective rectifier configuration is attributable to the British circuit genius, Peter Baxandall. Rectifier reference bias comes from the same asymmetrical source used by the peak control circuitry. This encourages a preponderance of positive-going program peaks in the compressor output. Midband attack time is fixed by R138 and C49. Release is through R139 to a “platform” established by C59 and a discharge resistance selected by IC43 per the PROGRAM DENSITY setting.

The LOW and HIGH bands have low-pass and high-pass characteristics, respectively. LOW and HIGH band compressor operation is identical to that described for the MID band, except that time constants are scaled appropriately.

Compression "Platform"

At the (MIN) PROGRAM DENSITY setting, IC43 selects R208 as a discharge path for C59. The DC control voltages from all three bands combine to charge C59 to an average of the three. This establishes a compression "platform," to which each band will release quickly, all three bands then further releasing slowly and simultaneously through R208. This gives the effect of independent, multiband action for program transients, but a slow and gentle broadband compression characteristic for the average value of the program.

At the most aggressive (MAX)setting of PROGRAM DENSITY, C59 is shorted directly to ground through IC43. This means that C59 cannot charge from DC compression-control voltages. There is no "platform" in this case, and each band of has its own fast release through either R120, R139 or R150, giving maximum multiband performance. Intermediate settings of PROGRAM DENSITY furnish compressor behavior between the two extremes.

VARIABLE EQUALIZATION (Schematic Sheet 1, Page 29)

The outputs of the three compressor sections are combined in summing stage IC34A. The MID band is fed through fixed resistance R127, but the LOW and HIGH bands are routed through selectable networks. IC33 and IC37 allow selection of five EQUALIZATON settings, both for LOW FREQ. and HIGH FREQ. This varies the gain of the LOW and HIGH bands in the final output "mix." Equalizer curves are shown on Page 5.

PEAK CONTROL (Schematic Sheet 2, Page 30)

Compressed program signals are applied to IC26B, which includes the previously-explained Q15/Q16 antediluvian gain-control element for linear peak limiting.

Q7 and Q8 serve a dual function. With emitters tied to stiff voltage sources, the base-emitter junctions *clip* the program signal at a predetermined and absolute "ceiling." In addition, collector current which also flows as the peaks are clipped is further amplified to generate a *limiter* control voltage for linear gain reduction.

Bias to establish this limiter threshold / clipping level is from voltage dividers tied to the power supply rails. Negative bias is fixed by R108 and R109. Positive bias, on the other hand, includes the POS. PEAKS control, R210. By elevating the positive bias, positive program peaks may be passed by the Processor with values which may be varied between 100% and 130% of negative peak values.

The PEAK PROCESSING selector controls analog switch IC14 to set peak limiter release time. The faster the release, (a lower value of resistance switched through IC14), the greater the incidence of program clipping and its attendant increase in perceived loudness.

At the two least-aggressive PEAK PROCESSING settings (1 and 2), a small DC bias from R43 and R44 is introduced into the limiter release equation. This assigns a fixed loss to the limiter circuit and reduces the total amount of peak level control to approximately 5dB.

Limiter release timing is programmed for the most useful working range of limiter/clipper action. The signal level at the output of IC26B which represents 100% symmetrical modulation is +5dBu.

FILTER OVERSHOOT COMPENSATION (Schematic Sheet 2, Page 30)

Sources of Overshoot

All low-pass filters exhibit a certain amount of overshoot and ringing when presented with complex input waveforms. Generally, the sharper the cutoff, the more pronounced the effect. Overshoots result from the elimination of higher-order input signal components which helped to define the signal peak amplitude before they were filtered out. Even a fully phase-corrected filter will exhibit overshoots, and a 9-pole “elliptic” filter, like the one used in the Model 235 Processor, can overshoot 3dB or more... perhaps *much* more!

Other systems of overshoot control permit the primary low-pass filter to overshoot, then isolate and re-introduce the overshoots to cancel themselves in the signal path. The patented overshoot compensator in the 235, on the other hand, pre-conditions the limited program signal *ahead* of the filter so there is little or no tendency for the filter to *generate* overshoots in the first place.

Phase-Lag and Recombining

As previously related, Q7 and Q8 constitute a “hard” clipper at the input of the compensation circuit and are biased to a point which represents 100%-modulation.

IC25B buffers the output of the Q7/Q8 clipper, and incorporates a gentle second-order rolloff above 15kHz. IC24B is an all-pass, phase-lag stage which time-displaces the fast leading and trailing edges of steep waveforms. This means that the primary characteristic of a program waveform which would normally *excite* filter overshoots is instead added to the waveform *amplitude*. A second clipper, Q22 and Q23, also biased to the 100%-modulation level, “strips” these displaced-and-added components from the program signal. IC22B compares the “stripper” input and output to recover the stripped-off components. These contain much of the program harmonic (high frequency) information, so we cannot afford simply to throw them away. By recombining these stripped-off program components with the stripped program signal *in opposite phase*, the spectral integrity of the program is maintained. This 180-degree displacement of certain program overtones is not discernible to the listener, but is quite effective in inhibiting filter overshoots.

For a more detailed discussion of this strange and wonderful filter overshoot compensation scheme, the reader is directed to U.S. Patent No. 4,737,725.

LOW-PASS FILTER (Schematic Sheet 2, Page 30)

The 9-pole, elliptic-function (Cauer) low-pass filter is an active version of the classic L-C design worked-out in Germany during the late 1940s, probably with a slide rule! The particular active configuration used in the 235 is sometimes called the “FDNR” because each of the legs to ground simulates a Frequency-Dependent Negative Resistance. Referring back to the classic L-C design, resistors in series with the signal replace series inductors, and each of the active circuits to ground simulates an inductor/capacitor series-resonant element.

A great “cookbook” which includes this and other filter circuits possibly useful to the DIY broadcaster is the *Electronic Filter Design Handbook* by Arthur B. Williams, published by McGraw-Hill. The reader is kindly directed to this source for a more informed discussion of how the FDNR circuit works than we could possibly deliver here, due not only to the limited scope of this Instruction Manual, but to our own marginal understanding of how these confounded things work!

IC22A buffers the output of the low-pass filter and IC21A provides phase inversion and gain to compensate for filter insertion loss. The signal level corresponding to 100% symmetrical modulation at the output of IC21A is +5dBu.

OUTPUT STAGE (Schematic Sheet 2, Page 30)

Q13 and Q14 form an output “safety” clipper biased to the same ceiling as the integrated limiter/clipper. Tight limiting and clipping, and effective filter overshoot control ensure that only very seldom will Q13 and Q14 act on the program signal. Nevertheless, they are included, “just in case.”

IC26A buffers the output signal and includes a gentle low-pass function for frequencies beyond the primary low-pass cutoff. IC27B and IC27C route the Processor input signal around the active circuitry in the PROOF mode.

The OUTPUT LEVEL control, R211, feeds gain stage IC25A. This stage includes current-booster transistors Q11 and Q12 to help drive interconnect cabling and transmitter input loads. CR19 and CR20 set bias for the two output transistors, and CR21 and CR22 give short-circuit protection. This is one-half of a “bridge” output configuration, the other half comprises unity-gain inverter IC23A, also with output-boosting discrete circuitry, to drive the opposite output polarity. The balanced program LINE OUTPUT is taken from between the two output amplifiers.

GAIN REDUCTION METERING (Schematic Sheet 3, Page 31)

DC control voltages from the AGC stage and the 3 bands of compression are fed to IC3B, a 1-of-4 analog multiplexer. Oscillator/counter IC2 sequences IC3, acting like a motor-driven rotary switch to commutate the four control-voltage inputs.

Control voltage represents the semi-log gain control transfer function. CR1 and CR2 translate this to a linear scale which is DC-offset by a reference voltage from IC1A. Thus the output of IC1B sits at approximately +3V with no gain reduction in effect, and drops toward ground as control voltage goes positive in response to gain reduction.

IC1B feeds display driver IC501 which drives the paralleled cathodes of the four LED readouts. Each LED readout has a common-anode connection fed by an emitter-follower. These four transistors are sequenced by IC3A to be in step with the sequenced control voltages from I3B. Thus a common log converter and display driver can serve the four, multiplexed gain-reduction displays.

COMMON CONTROL CIRCUITRY (Schematic Sheet 3, Page 31)

The 235 makes efficient use of a device called a “PIC,” or Peripheral Interface Controller, IC8 on the Schematic. This is a simple, single-chip microcontroller meant for elementary logic and uncomplicated control functions. We program it to perform certain routines dealing with front-panel buttons and indicators, and RS-232 serial communications.

IC9 converts the six panel button closures into a 3-bit binary address. The PIC keeps track of the various buttons pressed and latches individual, 3-bit binary output commands for LOW FREQ. and HIGH FREQ. EQUALIZATION, PROGRAM DENSITY and PEAK PROCESSING settings. The 3-bit outputs are also paralleled to a series of decoders which light the respective LED indicator strings for these four functions.

Switch S2, located on the rear panel of the 235, enables two operating modes in addition to local, front-panel control of the Processor.

In PROOF, processing circuitry is bypassed and the 235 becomes a unity-gain amplifier with flat frequency response. The PIC not only re-routes signal path circuitry, but flashes front-panel indicators to alert the operator that the unit is in PROOF.

In the REMOTE position, the PIC locks-out the front-panel buttons and instead responds to RS-232 serial commands for setting processing parameters. IC7 is an RS-232 level translator, buffering the serial data send and receive lines from the PIC.

POWER SUPPLY (Schematic Sheet 2, Page 30)

Model 235 circuitry utilizes ±9-volt supplies for op-amps and other linear circuitry, and a +5-volt supply for digital logic. These three sources are each regulated by a “3-terminal” linear voltage regulator; IC4 for +9 volts, IC6 for –9 volts, and IC5 for +5 volts.

The power transformer, T1, has dual primary windings which may be switched in parallel or in series to accommodate 115V or 230V mains, respectively.

Section VI

APPENDIX

The following section of this Manual contains Parts Lists and Schematic Diagrams for the Model 235, and an explanation of Inovonics' Warranty Policy.

PARTS LIST

EXPLANATION OF PARTS LISTINGS

This section contains listings of component parts used in the Inovonics 235 AM Broadcast Audio Processor. These are listed either *en-masse*, or by schematic component reference designation. The listing may, or may not, specify a particular manufacturer. When no manufacturer is called-out, the term "open mfgr." advises that any manufacturer's product is acceptable, so long as it carries the proper generic part number.

If a particular component is not listed at all, this means that we do not consider it a typical replacement item. Should you need to order an unlisted part, call, write or FAX the factory with a brief description. We'll do our best to figure out what you need and get it on its way to you quickly.

PARTS LISTING

Unless specifically noted by component reference designation below, **capacitors** are specified as follows:

a) **100pF to 0.47µF** are of the metalized mylar or polyester variety. Whole number "P" values are picofarads, decimal values are microfarads, ±5%, 50VDC or better. The style used in the 540 is the "minibox" package with a lead spacing of 0.2 inch. **Preferred part:** Wima MKS-2 or FKC-2 series. **Alternates:** CSF-Thompson IRD series, or Roederstein KT-1808 or KT-1817 series.

b) **1.0µF and above** are radial-lead electrolytics, value per schematic, 25VDC; (open mfgr.).

C1,2	Capacitor, Ceramic Disc "Safety" Mains Bypass, .0047µF, 440VAC; Murata/Erie DE7150 F 472M VA1-KC (preferred)
C4,5	Capacitor, Electrolytic, axial leads, 1000µF, 35VDC; (open mfgr.)
C15	Capacitor, Memory Back-Up, 1 Farad, 5.5VDC; (open mfgr.)
C21-24, 26,29-33	Capacitor, "High-Q," .0033µF, 2.5%, 100VDC; Wima FKC-2 (Polycarbonate) preferred, any equivalent *must* have similar, very-low-loss characteristics.
C38,39	Capacitor, Electrolytic, radial leads, 220µF, 6VDC; (open mfgr.)
CR1,2,11-29	Diode, Silicon Signal; (open mfgr.) 1N4151 or equiv.
CR3-10	Diode, Silicon Rectifier; (open mfgr.) 1N4005
CRES1	Ceramic Resonator, 4MHz; Mouser 520-ZTT400MG

F1	Fuseholder, PC-mounting; Littlefuse 345-101-010 with 345-101-020 Cap for ¼-inch (U.S.) fuses, or 345-121-020 Cap for 5mm (European) fuses. (Fuse is normal “fast-blow” type in value specified on rear panel with reference to mains supply.)
I501	LED Indicator, pastel red, T-1 package; Stanley MVR 3378S
I502	LED Indicator, pastel green, T-1 package; Stanley MPG 3878S
I503,504,505	10-Segment LED-bar display module, green; Kingbright DC-10GWA
I506	10-Segment LED-bar display module, yellow; Kingbright DC-10YWA
I507,508,509	10-Segment LED-bar display module, red; Kingbright DC-10EWA
IC1,12,13, 17-26,28-32, 34,36-41	Integrated Cct.; (open mfgr.) LF353N
IC2	Integrated Cct; (open mfgr.) CMOS 4060B
IC3	Integrated Cct; (open mfgr.) CMOS 4052B
IC4,5	Integrated Cct.; (open mfgr.) LM317-T (Uses Aavid 574602 B03700 Heat Fin)
IC6	Integrated Cct.; (open mfgr.) LM337-T (Uses Aavid 574602 B03700 Heat Fin)
IC7	Integrated Cct.; Maxim MAX232
IC8	Integrated Cct.; *SPECIAL FACTORY-PROGRAMMED “PIC,”* type 16C62A. Order by designation, reference Model 235.
IC9	Integrated Cct.; (open mfgr.) 74HC148
IC10,11,15,16	Integrated Cct.; (open mfgr.) 74HC138
IC14,33,37,43	Integrated Cct; (open mfgr.) CMOS 4051B
IC27,42	Integrated Cct; (open mfgr.) CMOS 4053B
IC501	Integrated Cct.; (open mfgr.) LM3914N
J1	AC Mains Connector, PC-mounting; Switchcraft EAC303
J3	Connector, 9-pin “D-Sub” female, PC-mounting; (open mfgr.)
Q1-4,6,7, 10,12,14,19, 20,22,26, 27,31,32,34	Transistor, NPN; (open mfgr.) 2N3904
O5,8,9,11, 13,21,23,28,33	Transistor, PNP; (open mfgr.) 2N3906
Q15-18,24, 25,29,30,35,36	Transistor, NPN; (open mfgr.) 2N5088

All resistors are specified as follows:

a) **Fixed resistors** with values carried to decimal places implying a 1% tolerance (*example:* 3.01K, 10.0K, 15.0K, 332K) are ¼-watt, 1% metal film type.

b) **Fixed resistors** with values typical of 5% tolerance (example: 220, 3.3k, 10K, 270K) are ¼-watt, 5% carbon film type.

c) **Multi-Turn Trimming Potentiometers** (front-panel adjustable) are Tokos RJC097P series, Beckman 89PR series, or equivalent “cermet” types.

S1	Switch, DPDT Slide, Voltage Selector; C&K V202-12-MS-02-QA
S2	Switch, SPST Toggle; C&K 7103-M-D9-A-B-E
S501-506	Switch, SPDT Momentary Pushbutton; ITT-Schadow D6-04-01, with F14-04 gray cap
S601	Switch, Power Rocker; Carling RA 911-RB-O-N
T1	Power Transformer, PC-mounting; Signal LP-20-600 or direct cross-reference

MAIL-ORDER COMPONENT SUPPLIERS

The following electronic component distributors have proven themselves reputable suppliers of small quantities of replacement parts for professional equipment.

> The temptation to use cross-referenced hobbyist or TV-shop ‘direct replacement parts’ (ha!) should be avoided!

Any semiconductor, IC, capacitor, resistor or connector used in the Model 235 is *probably* available from one or more of these firms. Each supplier publishes a full-line catalog, available free for the asking. Minimum-order restrictions may apply; and export orders may be difficult.

Mouser Electronics — Call (800) 346-6873

Digi-Key Corporation — Call (800) 344-4539

ACTIVE (div. of Future Electronics) — Call (800) 677-8899

Allied Electronics (div. of Avnet) — Call (800) 433-5700

Schematic Sheet 1
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Schematic Sheet 2
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Schematic Sheet 3
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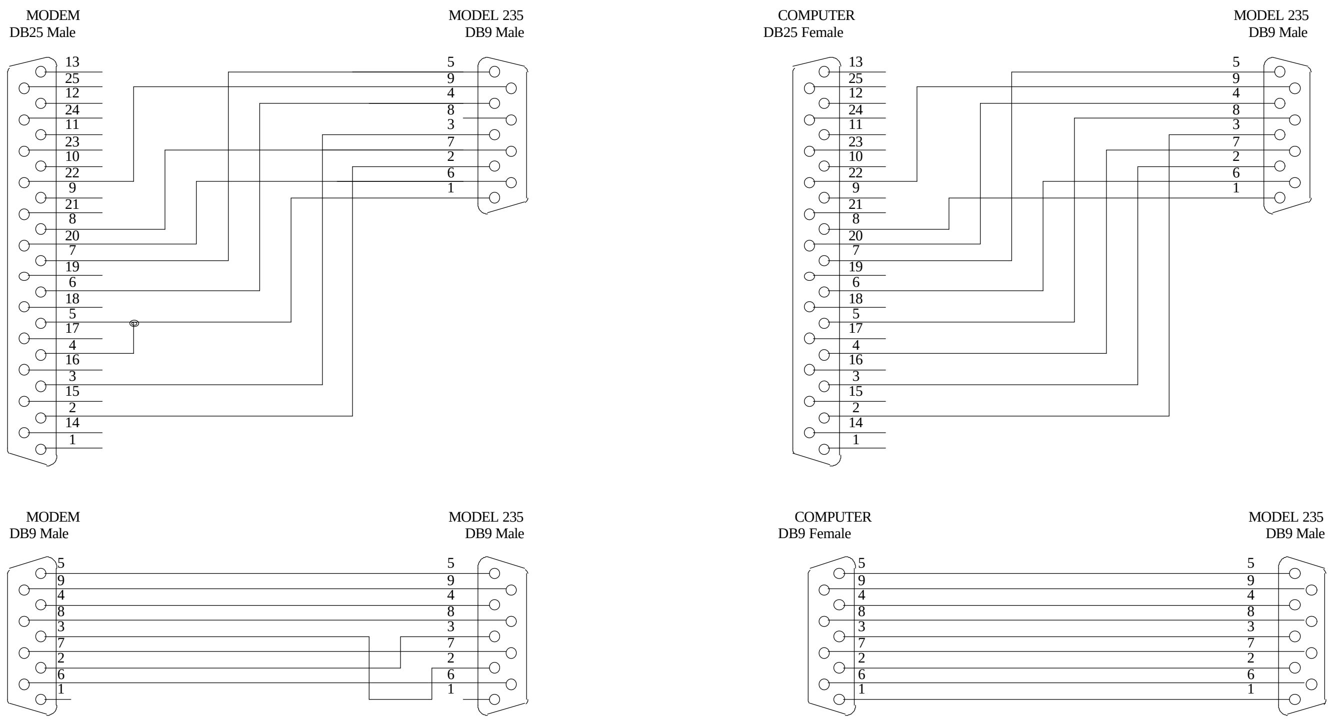

Interconnect Cables — Model 235 Processor to Computer or Modem

Schematic Sheet 4

INOVONICS WARRANTY

I **TERMS OF SALE:** Inovonics products are sold with an understanding of "full satisfaction"; that is, full credit or refund will be issued for products sold as new if returned to the point of purchase within 30 days following their receipt, provided that they are returned complete and in an "as shipped" condition.

II **CONDITIONS OF WARRANTY:** The following terms apply unless amended *in writing* by Inovonics, Inc.

A. Warranty Registration Card supplied with product *must* be completed and returned to Inovonics within 10 days of delivery.

B. Warranty applies only to products sold "as new." It is extended only to the original end-user and may not be transferred or assigned without prior written approval by Inovonics.

C. Warranty does not apply to damage caused by misuse, abuse, accident or neglect. Warranty is voided by unauthorized attempts at repair or modification, or if the serial identification has been removed or altered.

III **TERMS OF WARRANTY:** Inovonics, Inc. products are warranted to be free from defects in materials and workmanship.

A. Any discrepancies noted within 90 days of the date of delivery will be repaired free of charge, or the equipment will be replaced with a new or remanufactured product at Inovonics' option.

B. Additionally, parts for repairs required between 90 days and one year from the date of delivery will be supplied free of charge. Labor for factory installation of such parts will be billed at the prevailing "shop labor rate."

IV **RETURNING GOODS FOR FACTORY REPAIR:**

A. Equipment will not be accepted for Warranty or other repair without a Return Authorization (RA) number issued by Inovonics prior to its return. An RA number may be obtained by calling the factory. The number should be prominently marked on the outside of the shipping carton.

B. Equipment must be shipped prepaid to Inovonics. Shipping charges will be reimbursed for valid Warranty claims. Damage sustained as a result of improper packing for return to the factory is not covered under terms of the Warranty and may occasion additional charges.